The American University in Cairo

CENTER OF NANOELECTRONICS & DEVICES

CND 201
ADVANCED ANALOG CIRCUITS
2023

Course Description

This course aims to introduce the trainees to the concept of design, analysis, and verification of schematic and layout of basic and advanced analog circuits including current mirrors, differential amplifiers, and op-amps (single-stage, two-stage, telescopic, and folded cascode) by utilizing standard design and testing steps for schematic (i.e. testbench, pole splitting, DC, AC, STB, and transient analysis) and layout (i.e. floor planning, fingers, multipliers, matching, latch-up, antenna error, PEX, and post-layout simulations). Moreover, students explore the process of using ideal and practical op-amps employing industrial CAD tools (Cadence virtuoso, and Caliber) to design useful analog circuits such as integrators, differentiators, comparators, precision rectifiers, Schmitt triggers, oscillators, Butterworth and Chebyshev responses of second-order filters including sallen key, and integrator-based biquads

Contact Hours

Credit Hours	Lecture Hours	Lab Hours	Student work	Total
6	24 (1.25x2)/week	21 (3x1)/week	48	93

Prerequisites

Introduction to Analog Electronics

Learning Outcomes

After successful completion of this course, the student will be able to:

1. Design and evaluate the schematic and layout of different types of:
   - Operational amplifiers (single-stage, two-stage, telescopic, and folded cascode),
   - linear and nonlinear circuits of op-amp (integrators, differentiators, comparators, precision rectifiers, Schmitt triggers),
   - Oscillators (Bistable and Astable), and
   - Analog filters (Butterworth and Chebyshev responses of second-order filters including sallen key, and integrator-based biquads).
2. Use advanced CAD tools (Cadence virtuoso, and Caliber) to design and simulate analog electronic circuits by utilizing standard design and testing steps for:
   - Schematic (i.e. testbench, pole splitting, DC, AC, STB, and transient analysis) and
   - Layout (i.e. floor planning, fingers, multipliers, matching, latch-up, antenna error, PEX, and post-layout simulations).

Course Materials

Textbook:

- Razavi, Behzad. Design of analog CMOS integrated circuits, 2005.
- Razavi, Behzad. Fundamentals of microelectronics. John Wiley & Sons, 2021.
- Adel S. Sedra, Kenneth C. Smith, Tony Chan Carusone, Vincent Gaudet, Microelectronic Circuits, 8th Edition, Oxford University Press.
- Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits. 4th Ed, McGraw-Hill Education.
- Gray, Paul R., et al. Analysis and design of analog integrated circuits. John Wiley & Sons, 2009.

References:

- Material is also derived from the IEEE Journal, Transactions, and the International Solid-state Circuits Conference (ISSCC) proceedings.

CAD Tools: Cadence flow including

- Virtuoso ADE suite
- Spectre
- Virtuoso Visualization
- ADE assembler editing (maestro)
- Calibre (nmDRC, nmLVS, xRC)

Course Project: By the end of this course the students are required to deliver a complete project (chosen from variety of proposals) assigned by the industry experts and university professors instructors.

Course Topics and Schedule

Week	Lecture	Lab
1	Operational amplifier fundamentals (Ideal Op-Amp) : (Amplifier fundamentals, The Ideal Op Amp, Differential and Common-Mode Signals, Basic op-amp configurations, and Differential and Common-Mode Signals)	Lab_1: Operational Amplifier Fundamentals
2	Ideal op-amp circuit analysis (Ideal Op-Amp): (The Summing Amplifier, The Difference Amplifier, The Differentiator, The Integrator, Current-to-Voltage Converters, Voltage-to-Current Converters, Current Amplifiers, and Instrumentation Amplifiers.	Lab_2: Design Single Stage Operational Amplifier & Current Mirror
3	The Two-Stage CMOS Op Amp (Transistor level): (DC Imperfection, Offset voltage, Bias and offset current, Bandwidth, Input Resistance, Output Resistance, Output Swing, Common-Mode Rejection Ratio, Common-Mode Input Range,	Lab_3: Design of aTwo-Stage Miller Compensated OTA

	Slew Rate, Power-Supply Rejection Ratio (PSRR), and Effect of Overdrive Voltages	
4	Layout: (General Layout Considerations, Design Rules, Antenna Effect, Analog Layout Techniques, Multi-finger Transistors, and Symmetry)	Lab_4: Matching, Floor planning, current mirror layout, and not gate layout automation.
5	Layout: (Shallow Trench Isolation Issues, Well Proximity Effects, Reference Distribution, Passive Devices, Interconnects, and Pads)	Lab_5: Design of Differential amplifier layout (back end)
6	Noise: (Root mean square, Noise Spectrum, Signal-to-Noise Ratio, Correlated and Uncorrelated Sources, White Noise, Resistor Thermal Noise, MOSFET Thermal Noise, Flicker Noise, Representation of Noise in Circuits, Noise in Common source, Noise in Differential Pairs	Lab_6: Design for Folded Cascode OTA Layout
7	Feedback: (Signal-Flow Diagram, The Closed-Loop Gain, Gain Desensitization, Bandwidth Modification, Nonlinearity Reduction, Types of Amplifiers, Return Mechanisms, Voltage-Voltage Feedback, Effect of Feedback on Noise	Lab_7: Operational Amplifier Validation.
8	signal generators: (general considerations, ring oscillators, lc oscillators, the cross-coupled lc oscillators, phase shift oscillator, amplitude control, wien-bridge oscillator, colpitts oscillator, voltage-controlled oscillators, tuning in ring oscillators, tuning in lc oscillators	Lab_8: Design of aTwo-Stage Miller Compensated OTA
9	nonlinear circuits: (voltage comparators, comparator applications, schmitt triggers, precision rectifiers, analog switches, peak detectors, logarithmic amplifier, and square root amplifier	Lab_9: Implementation of a Signal Generator (an astable multivibrator with -ve and +ve feedback)
10	Filters: (general considerations, filter characteristics, classification of filters, filter transfer function, and second-order filters)	Lab_10: Active Filters (Chevycheb and Butterworth technique of Sallen and Key Filter)
11	Active Filters: (Sallen and Key Filter, Integrator-Based Biquads, Biquad developed by Tow and Thomas, Butterworth and Chebyshev Response)	